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For:

LED Array Architecture For High Resolution Printbars

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an LED printing device and, more particularly, to a high resolution LED array bar.

2. Brief Description of Related Developments

It is common to use light emitting diode (LED) bars in printing devices. LED bars provide reliable and controllable light sources. The bars are generally comprise a plurality of light sources, i.e., pixels that can be activated and deactivated (pulsed) to emit short bursts of light at a high rate of speed. Each light burst is used to create a particular portion of a printed symbol or character. The more often a pixel is pulsed, the more often a symbol or character portion will be imaged, thus providing greater detail and higher resolution printing. Therefore, for the printing to be completed within a commercially reasonable time with high resolution, it is necessary to have a high rate of pulsing.

LED bars are manufactured in different segment, or chip, sizes. Segment size depends on the number of pixels within the segment. Two popular numbers of pixels per segment are 64 pixels and 128 pixels. At 424.26 spot per inch (SPI) these segments would be 3.832 and 7.663 mm respectively. The respective lengths are determined by

dividing the number of pixels by the spot per inch requirement and converting the quotient to millimeters. For example:

$$64(\text{pixels}) \times \frac{1}{424.26(\text{spi})} = .1509 \text{ in} \times 25.4 \frac{\text{mm}}{\text{in}} = 3.832 \text{ mm}$$

$$128(\text{pixels}) \times \frac{1}{424.26(\text{spi})} = .3017 \text{ in} \times 25.4 \frac{\text{mm}}{\text{in}} = 7.663 \text{ mm}$$

- 5 The technologies that create linear arrays of LED's, composed of discrete chips placed side-by-side, have evolved to where 600 SPI densities are easily achievable. In fact, this density is found in most printers using LED bars. Higher densities are also possible, and a 1200 SPI
10 bar is on the market.

Evaluation of a 1200 SPI bar revealed an inconsistent pitch. The distance between adjacent pixels on different chips was large by more than 4.3 μm or 20% of the pitch.
see Figure 1. (Pam)
This much error causes undesirable banding on prints.

- 15 Clearly, the technology that creates LED's has improved to where 1200 SPI LED's are possible, but the technology that places the chips has remained at 600 SPI.

- Five design rules govern the creation of true 1200 SPI arrays. State-of-the-art arrays, represented by the
20 evaluated bar, fail to meet all five. The rules are: (1) Emitters can not be too large. Large emitters have optical and electrical crosstalk. (2) Emitters can not be too small. Small emitters inefficiently generate light so require high current and produce high temperatures.
25 (3) Emitters cannot be too close to the chip edge. Close emitters develop an infant mortality caused by fractures created when the chip is diced from the wafer. (4) The

gap between chips can not be too small. Small gaps give a high probability that a chip will contact its neighbor and fracture during placement into array. Furthermore, the gap allows thermal expansion. If chips
 5 contact during expansion, they fracture or break the adhesive. (5) The pitch must be consistent or else banding occurs.

Using existing practices, rules (1) and (2) are met as evidenced by the chips of the evaluated bar and by other
 10 experimental chips. Chips can be made of viable 10.5 μm width LED's. Rules (3), (4), and (5) remain problematic though. They are mutually exclusive. Chips can be diced no closer than 5 μm from the emitter. Placement is no
 15 better than $\pm 11 \mu\text{m}$ for engineering work and closer to $\pm 2.5 \mu\text{m}$ for production work. So, 1200 SPI chips can be placed on-pitch as shown in Figure 2 or over-pitch as shown in Figure 3. On-pitch yields a gap of 0.7 μm . This exceeds even engineering accuracies so is impractical. The
 20 smallest over-pitch yields a spacing of 25.5 μm which is 4.3 μm greater than the ideal pitch of 21.2 μm . The evaluated bar uses it, but of course, with the defect.

Thus, it would be helpful to be able to form a 1200 SPI LED array with a consistent pitch while minimizing the array size and distance between adjacent chips.

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SUMMARY OF THE INVENTION

The present invention is directed to a method of forming a high resolution LED array. In one embodiment the method comprises providing a plurality of LED chips to form the LED array. An electrode of an LED located at each end of each chip is inward biased by a predetermined amount. The size of each LED chip is reduced by removing, at each end of each chip, an amount of chip material substantially equal to the predetermined amount. The array is formed by placing each chip end to end with a gap between each chip, wherein the gap is suitably large for placement accuracies in a consistent pitch of approximately 21.2 μm is maintained between each LED on each chip.

In another aspect, the present invention is directed to a high resolution LED printbar. In one embodiment the high resolution LED printbar comprises a plurality of LED chips butted together with a gap between adjacent LEDs to form an array. Each LED chip generally comprises a plurality of LEDs where each LED is adapted to generate an emitted light. A center electrode extends from each LED and is adapted to electrically connect the LED to a wired bond pad. The center electrode is generally positioned over an emitting side of the LED and a centroid of light from each LED is centered over the LED. An LED at each end of the chip has an electrode that is inward biased over each respective end LED. A centroid of emitted light from each end LED is positioned closer to an outer edge of the chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and other features of the present invention are explained in the following description, taken in connection with the accompanying drawings, wherein:

5 FIG. 1 is a graph illustrating the differences in pitch between pixel spacing in a conventional 1200 SPI LED bar.

FIG. 2 is an illustration of 600 SPI architecture applied to a 1200 SPI LED array bar.

10 FIG. 3 is an illustration of 1200 SPI LED chips moved closer together to eliminate pitch error.

FIG. 4 is a graph comparing the emission performance of a center electrode, ~~and a side electrode.~~ (pm)

FIG. 5 is a graph comparing the emission performance of a side electrode.

15 FIG. 6 is an illustration of one embodiment of a 1200 SPI LED chip architecture incorporating features of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(s)

20 Referring to Fig. 1, there is shown a perspective view of a system 10 incorporating features of the present invention. Although the present invention will be described with reference to the embodiment shown in the drawings, it should be understood that the present
25 invention can be embodied in many alternate forms of embodiments. In addition, any suitable size, shape or type of elements or materials could be used.

Referring to Fig. 6, the present invention generally comprises a linear LED array having a consistent pitch between adjacent pixels that satisfies the general design rules for 1200 SPI LED arrays. The light intensity of the end LED devices on each chip of a printhead in an array is shifted in order to make the light appear closer to the end of the array than it actually is. This allows the chip to be diced closer to the light centroid and the chips in the array can be stitched or mounted closer together. As shown in Fig. 6, the electrode 52 on the end LED 56 is inward biased to move the centroid of the emitted light closer to the chip edge. The centroid of LED 56 is no longer centered over the LED. This allows the gap 58 between chips 51 and 53 to be larger than the gap 27 shown in Fig. 2, while substantially maintaining the correct or ideal distance between adjacent pixels on different chips. The LED array of the present invention eliminates the ~~spikes (ARM)~~ ^{spikes (ARM)} shown in Fig. 1 and removes the associated banding. It is a feature of the present invention to provide a linear 1200 SPI LED array with a constant pitch of 21.2 μm and a minimal gap between LED chips without fracture or contact between adjacent chips.

A linear LED array generally comprises a series of LED chips. For example, referring to Fig. 2, the LED array 20 comprises at least two LED chips 22. Each LED chip 22 generally comprises a plurality of LED's 26. Each LED 26 is affixed to the LED chip 22 in a conventional fashion. As shown in Fig. 2, each LED 26 has an associated center electrode 28 that can be used to electrically connect the LED 26 to a wire bond pad 24 for example. The center electrode shown in Fig. 2 produces an emission centroid centered over the LED 26. The electrode 28 blocks light

at the center but does not change the centroid of the light.

Fig. 2 is an illustration of a typical 600 SPI architecture applied to 1200 SPI. In order to maintain at least a $5\mu\text{m}$ buffer zone between the end LED 21 and the chip edge 23, as well as maintain at least a $5\mu\text{m}$ gap 27 between chips 22a, 22b, the pitch 29 between adjacent pixels on different chips is significantly larger than the average pitch 25. This is undesirable. The LED bar evaluated to produce the graph of Fig. 1 is similar to the architecture shown in Fig. 2. Fig. 1 is a graph of the differences in pixel spacing of a 1200 SPI LED bar manufactured by Okidata. The average spacing on pitch between pixels on the same chip is $21.2\mu\text{m}$. However, the spacing of adjacent pixels on different chips is $4.3\mu\text{m}$ over-pitch. The ~~spikes~~ ^{spikes (nm)} shown on the graph occur at every chip boundary.

In order to reduce the pitch error, the LED chips can be moved closer together as shown in Fig. 3. However, in order to eliminate the pitch error, as illustrated in Fig. 2, the chips 22a and 22b would have to be spaced apart or have a gap 34 of $0.7\mu\text{m}$. This is not realistic given the capabilities of existing chip placement machines. Additionally, such close placement would result in adjacent chip collisions and fracture. In addition, such a small gap does not provide room for thermal expansion of the chips.

As LED size decreases, structures composing the LED, such as the LED chips 22 shown in Fig. 2 for example, increasingly affect the emitted light profile. For

example the top electrode 28 shown in Fig. 2 becomes a factor because its size does not scale proportionately. Gold deposition and current capacity constraints limit the size of the electrode. The ~~side~~ electrode over a 1200 SPI LED covers a greater percentage ~~of~~ the LED emitter area, absorbs a greater percentage of the light and affects the emitted light profile more.

The present invention is used to vary the emitted light profile of an LED. If the electrode 28 is moved toward a side of the emitter, as shown in Fig. 6, the side electrode 52 blocks light at its side so it pushes the centroid toward the opposite side from the position of the side electrode 52. Fig. 4 shows 1200 SPI-sized LEDs with two electrode configurations.

Plots 41 and 43 of Figs. 4 and 5 are micrographs of 1200 SPI-sized LEDs. The bottom plots 42 and 43 are corresponding near field emission scans overlaid on the LED region. In plot 42 the emission line is 423 and the LED profile line is 421. In plot 44, the emission line is 441 and the LED profile line is 443. The side electrode 52 of Fig. 6 produces a centroid ~~right~~ of center (pushes light toward edge of chip). As shown in Figs. 4 and 5, the LED profile centroid of each plot 42, 44 is at 20.8 μm . The emission centroid produced by the center electrode LED 26 of Fig. 2 is at 20.8 μm . The emission centroid produced by the side electrode LED 56 of Fig. 6 is at 18.2 μm . The side electrode 52 of Fig. 6 moves the centroid ~~2.6~~ μm relative to the LED 56.
 2.6 (pm)

The present invention applies a side electrode configuration to minimize the gap 58 between adjacent LED chips 51 while maintaining a constant pitch between

pixels. For example, as shown in Fig. 6, the side electrode 52 biases the centroid towards the edge by approximately 2.6 μm . The emitter 56 is placed inwards by the same amount to maintain the correct spacing with other pixels 51a-51d on the chip 51. Moving or shifting the emitter 56 inwards allows the chip 51 to be smaller by the same amount. This is done to both sides of each chip in the array. The gap 58 between adjacent arrays is widened by approximately twice the amount that the emitter 56 is shifted, or as shown in Fig. 6, 5.2 μm . As shown in Fig. 6, a gap 58 of approximately 6.4 μm can be established between adjacent chips 51 and 53, which is suitably large for chip placement accuracies and thermal expansion. The configuration shown in Fig. 6 also complies with the other form design rules for 1200 SPI arrays, and achieves a true 1200 SPI array with a consistent pitch of approximately 21.2 μm . Although the disclosed embodiments are described herein with reference to a 1200 SPI array, the features of the disclosed embodiments can be applied to any high resolution imager or scanner made by butting IC's to form an array.

In alternate embodiments, the electrode configuration shown in Fig. 6 can require tuning for different LED material sets and wavelengths because the side electrode profile 44 shown in Fig. 4 implies that light transmission through a material could also be a factor. The power of the asymmetrical pixel could also be adjusted so that its width is comparable to others.

By shifting the electrode of an LED to the side of the emitter, the light centroid is pushed toward the opposite side. This shift in light intensity can make the end LED

devices on each chip of a printhead in an array appear closer to the end than they actually are. This allows the chips to be smaller and the gap between chips to be widened, while maintaining a constant pitch of for example, 21.2 μm between the pixels of the chips in the array. The resulting gap overcomes the problems associated with a smaller gap, such as chips colliding, arm fracture, or chip placement errors. The present invention provides 1200 SPI and greater linear arrays with substantially no pitch errors at chip junctions and better image quality characteristics.

It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances which fall within the scope of the appended claims.